

We claim:

1. A programmable resistance memory element, comprising:

a first dielectric material having a sidewall surface;

a conductive layer formed over said sidewall surface;

5 a second dielectric material formed over said conductive layer, wherein an edge of said conductive layer is exposed;

a third dielectric material formed over said edge, said third dielectric material having a opening formed therethrough uncovering a portion of said edge; and

10 a programmable resistance material disposed in said opening and in communication with said edge.

2. The memory element of claim 1, wherein said opening has a lateral dimension less than a photolithographic limit.

3. The memory element of claim 1, wherein said opening is a trench.

4. The memory element of claim 1, wherein said edge is annular.

5. The memory element of claim 1, wherein said edge is linear.

6. The memory element of claim 1, wherein said conductive layer is a sidewall layer.

7. The memory element of claim 1, wherein said conductive layer is a sidewall spacer or liner.

8. The memory element of claim 1, wherein said memory material is a phase-change material.

9. The memory element of claim 1, wherein said memory material comprises a chalcogen element.

10. A programmable resistance memory element, comprising:  
a first layer of a conductive material;  
a second layer of a programmable resistance material, wherein an edge of said first layer is adjacent to an edge of said second layer.

11. The memory element of claim 10, wherein substantially all electrical communication between said conductive material and said programmable resistance material is through said edge of said first layer and said edge of said second layer.

12. The memory element of claim 10, wherein said first layer is a sidewall layer.

13. The memory element of claim 10, wherein said first layer is a conductive sidewall spacer or liner.

14. The memory element of claim 10, wherein programmable resistance memory material comprises a phase-change material.

5 15. The memory element of claim 10, wherein said programmable resistance memory material comprises a chalcogen.

16. A programmable resistance memory element, comprising:

a layer of a conductive material;

10 a trench or pore of programmable resistance memory material adjacent to an edge of said layer of conductive material.

17. The memory element of claim 16, wherein substantially all electrical communication between said conductive material and said programmable resistance material is through said edge.

18. The memory element of claim 16, wherein said layer is a sidewall layer.

20 19. The memory element of claim 16, wherein said layer is a sidewall spacer or liner.

20. The memory element of claim 16, wherein programmable resistance memory material comprises a phase-change material.

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21. The memory element of claim 16, wherein said programmable resistance memory material comprises a chalcogen.

22. A method of forming an opening in a layer of a first material of a semiconductor device:

providing said layer of said first material;

forming a layer of a second material over said layer of said first material;

forming a layer of a third material over said layer of said material;

forming a sidewall surface in said layer of said third material;

forming a sidewall spacer of a fourth material on said sidewall surface;

forming a layer of a fifth material over said sidewall spacer and an exposed portion of said layer of said second material;

removing a portion of said fifth material to expose said sidewall spacer;

removing said sidewall spacer;

removing a portion of said layer of said second material exposing said layer of said first material; and

removing a portion of said layer of said first material to form said opening.

23. The method of claim 22, wherein said first material comprises a dielectric.

25. The method of claim 22, wherein said first material comprises an oxide, said second material comprises a nitride, said third material comprises an oxide, said fourth material comprises polysilicon, and said fifth material comprises an oxide.

25. The method of claim 22, wherein forming said sidewall spacer step comprises the step of:

forming a layer of said fourth material over said sidewall surface of said layer of said third material;

removing a portion of said layer of said fourth material.

26. The method of claim 25, wherein said removing step comprises the step of anisotropically etching said layer of said fourth material.

27. The method of claim 22, wherein said removing a portion of said layer of said fifth material step is a chemical mechanical polishing step.

28. The method of claim 22, further comprising the step of:

after said removing a portion of said layer of said fifth material, etching a portion of said fifth material and said third

material.

29. The method of claim 22, further comprising the step of:

after said removing a portion of said second material,

5 removing said third and said fifth materials.

30. The method of claim 22, further comprising the step of:

after forming said opening in said layer of said first material, removing layer of said second material.

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31. The method of claim 22, further comprising the step of:

after said forming said sidewall spacer and before said forming said layer of said fifth material over said sidewall spacer, removing said layer of said third material.

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32. The method of claim 22, further comprising the steps of:

after removing said portion of said layer of said second material but before forming said opening in said layer of said first material,

20 removing a portion of said layer of said first material to form a recess in said layer of said first material; and removing said layer of said second material.

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33. A method of forming an opening in a layer of a first material of a semiconductor device:

providing said layer of said first material;

forming a layer of a second material over said layer of said material;

forming a sidewall surface in said layer of said second material;

forming a sidewall spacer of a third material on said sidewall surface;

forming a layer of a forth material over said sidewall spacer and an exposed portion of said layer of said first material;

removing a portion of said forth material to expose said sidewall spacer;

removing said sidewall spacer; and

removing a portion of said layer of said first material to form said opening.

34. The method of claim 33, wherein said first material comprises a dielectric.

35. The method of claim 33, wherein said first material comprises an oxide, said second material comprises a nitride, said third material comprises polysilicon, said forth material comprises an oxide.

36. A method of forming a programmable resistance memory element,  
comprising the steps of:

providing a layer of a conductive material;

forming a layer of a first material over said layer of said  
5 conductive material;

forming a layer of a second material over said layer of said  
first material;

forming a layer of a third material over said layer of said  
material;

10 forming a sidewall surface in said layer of said third  
material;

forming a sidewall spacer of a forth material on said  
sidewall surface;

forming a layer of a fifth material over said sidewall spacer  
15 and an exposed portion of said layer of said second material;

removing a portion of said fifth material to expose said  
sidewall spacer;

removing said sidewall spacer;

removing a portion of said layer of said second material  
20 exposing said layer of said first material;

removing a portion of said layer of said first material to  
form said opening; and

depositing a programmable resistance material into said  
opening, said programmable resistance material in communication  
25 with said layer of said conductive material.

37. The method of claim 36, wherein said providing said layer of said conductive material comprises the steps of:

providing a first layer of a dielectric material;

forming a sidewall surface in said first layer of said dielectric material;

forming said layer of said conductive material over said first layer of said dielectric material; and

forming a second layer of a dielectric material over said layer of said conductive material; and

exposing an edge of said layer of said conductive material.

38. The method of claim 36, wherein said layer of said conductive material is a sidewall spacer or an sidewall liner.

39. The method of claim 36, wherein said layer of said first material comprises a dielectric.

40. The method of claim 36, wherein said first material comprises an oxide, said second material comprises a nitride, said third material comprises an oxide, said fourth material comprises polysilicon, said fifth material comprises an oxide.

41. A method of forming a programming resistance memory element, comprising the steps of:

providing a layer of a conductive material;

forming a layer of a first material over said layer of said  
5 conductive material;

forming a layer of a second material over said layer of said  
material;

forming a sidewall surface in said layer of said second  
material;

10 forming a sidewall spacer of a third material on said  
sidewall surface;

forming a layer of a forth material over said sidewall spacer  
and an exposed portion of said layer of said first material;

removing a portion of said forth material to expose said  
15 sidewall spacer;

removing said sidewall spacer;

removing a portion of said layer of said first material to  
form said opening; and

20 depositing a programmable resistance material into said  
opening, said programmable resistance material in communication  
said layer of said conductive material.

42. The method of claim 41, wherein said providing said layer of  
said conductive material comprises the steps of:

25 providing a first layer of a dielectric material;

forming a sidewall surface in said first layer of said dielectric material;

forming said layer of said conductive material over said first layer of said dielectric material; and

5 forming a second layer of a dielectric material over said layer of said conductive material; and

exposing an edge of said layer of said conductive material.

43. The method of claim 41, wherein said layer of said conductive  
10 material is a sidewall spacer or an sidewall liner.

44. The method of claim 41, wherein said first material comprises a dielectric.

15 45. The method of claim 41, wherein said first material comprises an oxide, said second material comprises a nitride, said third material comprises polysilicon, said forth material comprises an oxide.